Contents

Preface **ix**

1 Introduction **1**
1.1 History of device simulation 8
1.2 History of process simulation 10
1.3 Evolution of TCAD 12
1.4 Process flow integration 13
1.5 TCAD and compact model 15
1.6 Parameter extraction 17
1.7 Statistical process control and yield analysis 18
1.8 Virtual wafer fabrication 19
1.9 Optimisation 20
1.10 TCAD for nanoelectronics 20
1.11 Interconnect 23
1.12 Summary 23
References 25

2 IC technology and TCAD tools **31**
2.1 Process simulation 32
2.1.1 Oxidation 33
2.1.2 Ion implantation 33
2.1.3 Diffusion 34
2.1.4 Lithography 35
2.1.5 Etching 37
2.1.6 Metallisation 37
2.2 Plasma processing 40
2.3 Chemical mechanical polishing 43
2.4 Synopsys TCAD Tools 44
2.5 SILVACO: TCAD simulation suite 46
2.5.1 ATHENA 47
2.5.2 ATLAS 47

2.6 Process-to-device simulation using SILVACO 48
2.6.1 Device generation 49
2.6.2 Device simulation 50
2.7 Simulation example: strained-Si MOSFET 54
2.8 Summary 56
References 58

3 Diffusion and oxidation of SiGe/SiGeC films 63
3.1 Boron out-diffusion 63
3.2 Diffusion: B in strained-SiGe 65
3.3 Diffusion: P and As in strained-SiGe 70
3.4 Dopant diffusion in SiGeC 75
3.5 Oxidation: SiGe/SiGeC films 79
3.5.1 Oxidation kinetics 80
3.5.2 Plasma oxidation of SiGe films 84
3.6 Summary 88
References 89

4 Strain-engineered MOSFETs 97
4.1 Scaling issues 100
4.2 Mobility-enhanced substrate engineering 102
4.2.1 Orientation-dependent mobility engineering 104
4.2.2 Mobility enhancement by process-induced stress 106
4.2.3 Mobility enhancement by substrate-induced strain 111
4.3 Channel engineering 117
4.4 Gate engineering 120
4.5 Strained-engineered CMOS technology 127
4.6 Layout engineering 132
4.7 Strain-engineered MOSFETs: simulation 136
4.8 Summary 143
References 143

5 SOI MOSFETs 153
5.1 Fabrication of SOI wafers 154
5.2 SOI devices 158
5.2.1 Partially depleted SOI transistors 160
5.2.2 Fully depleted SOI transistors 162
5.3 Double-gate MOSFET 163
5.4 TCAD simulation of SOI devices 165
5.5 Simulation using MASTAR 168
5.6 Strained-Si MOSFETs on SOI 171
5.6.1 Simulation of SSGOI MOSFETs 173
5.6.2 MC simulation of sSOI MOSFETs 180
5.7 Modelling of multi-gate SOI devices 184
5.8 Summary 188
References 189

6 Heterostructure bipolar transistors 195
6.1 The first SiGe transistor 199
6.2 Issues related to heterostructure 200
6.3 SiGe materials 204
6.3.1 UHVCVD growth of SiGe films 206
6.4 Physics of SiGe HBTs 208
6.5 Figures of merit of SiGe HBTs 211
6.6 Simulation of SiGe HBTs 213
6.7 Transit time in SiGe HBTs 219
6.8 SiGe HBTs at low temperature 220
6.9 Summary 224
References 227

7 SiGe/SiGeC HBT technology 233
7.1 SiGe-BiCMOS technology 238
7.2 IBM SiGe-BiCMOS technology 240
7.2.1 Base-during-gate process 240
7.2.2 Base-after-gate process 243
7.3 SiGe HBTs on SOI 245
7.4 Complementary SiGe HBT technology 247
7.5 SiGeC HBT technology 249
7.6 TCAD: SiGe/SiGeC BiCMOS process 254
7.7 Summary 259
References 260

8 MOSFET: compact models 267
8.1 Charge-based MOSFET models 268
8.2 Surface-potential based MOSFET models 271
8.2.1 SP model 273
8.2.2 HiSIM 275
8.2.3 MOS model 11 275
8.2.4 EKV model 277
8.3 Model evaluation 279
8.4 Modelling of SOI MOSFETs 280
8.5 Modelling of heterostructure MOSFETs 281
8.6 RF MOS modelling 285
8.7 Large-signal MOSFET models 287
8.8 Summary 295
References 295

9 HBT: compact models 301
9.1 Advanced models 304
9.2 VBIC model 305
9.3 MEXTRAM model 310
9.4 The HICUM model 312
9.5 Parameter extraction 314

9.6 Extraction algorithm 316
9.7 VBIC model implementation in SPICE 323
9.8 TRADICA 332
9.9 Scalable modelling: SiGe/SiGeC HBTs 333
9.10 Role of TCAD 339
9.11 Summary 341
References 343

10 Design and simulation of high-speed devices 351
10.1 SiGe vs. GaAs HBTs 354
10.2 Device simulation 356
10.2.1 Device simulators 357
10.3 Material parameters 359
10.3.1 Bandgap and bandgap narrowing 361
10.3.2 Conduction band density of states 365
10.3.3 Valence band density of states 366
10.3.4 $Si_{1-x}Ge_x$ mobility 368
10.3.5 Saturation velocity 372
10.3.6 Generation and recombination 373
10.3.7 Impact ionisation 375
10.4 Simulation of III–V devices 376
10.5 Comparison of HBTs 384
10.6 RFMOS vs. HBTs 390
10.7 Summary 394
References 397

11 Passive components 409
11.1 Inductor 411
11.1.1 Inductor model description 414
11.1.2 Quality factor 417
11.2 Parameter extraction 418
11.3 Inductor simulation 421
11.3.1 ASITIC 423
11.4 Active inductors 425
11.5 Capacitors 427
11.6 Varactor 429
11.7 Resistor 430
11.8 Interconnects 431
11.9 Summary 434
References 434

Index 439