The Institution of Engineering and Technology

IET National Travel Post-Trip Report

CPE Annual Conference 2026 | University of Edinburgh

Farhan Tanvir, MEng Electronic and Electrical Engineering, University of Leeds

Pulsed Power at a National Platform

The Centre for Power Electronics (CPE) Annual Conference is one of the few UK forums where wide-bandgap semiconductor research meets real national infrastructure problems. The IET National Travel Award let me attend as a presenting delegate and put work that would otherwise stay in a university laboratory in front of that kind of audience.

The research I presented at the Nucleus Building, University of Edinburgh, on 7 and 8 July 2026 is the technical core of my final-year MEng project at the University of Leeds, supervised by Dr Benjamin Chong and developed with the AWE Nuclear Security Technologies.

The aim is specific: to design a solid-state replacement for the legacy gas-discharge and thyristor peaking circuits still in service at the AWE Orion laser facility. That legacy assembly has to be consolidated into a single solid-state topology that removes the electromagnetic interference (EMI) its operation generates, interference that currently threatens the validity of the facility's diagnostic data.

Getting there by rail

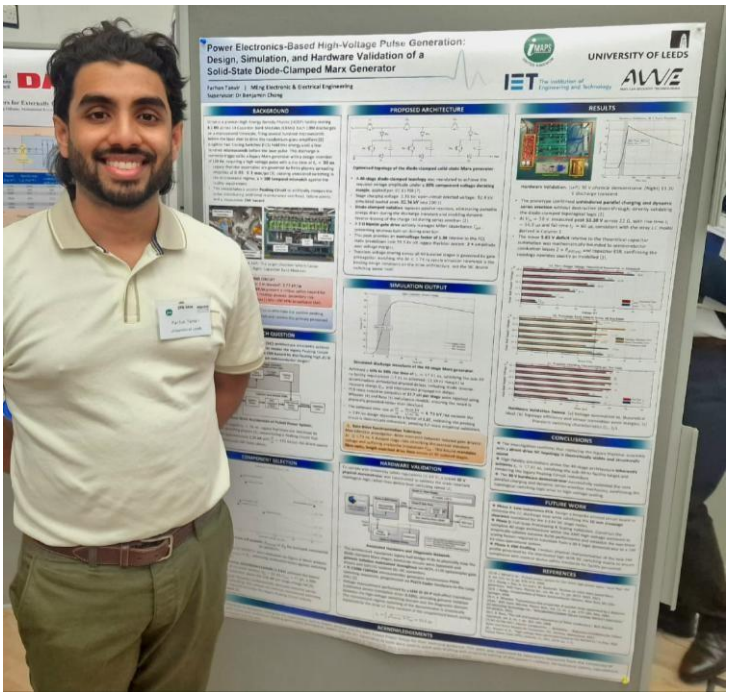
I travelled to Edinburgh by rail rather than driving or flying. The train cut the carbon footprint of the trip substantially, which felt right for a conference whose sessions kept returning to sustainable power conversion, the thermal management of high-frequency switching, and building infrastructure that lasts. My rail travel and registration were supported by the iMAPS/CPE organisers alongside the IET award.

Technical Focus

The programme was built around the practical problems of putting Silicon Carbide (SiC) and Gallium Nitride devices to work in demanding power electronics. Sessions covered high-frequency switching dynamics, keeping parasitic loop inductance low in PCB layouts, and tuning bipolar gate-drive design to suppress the Miller effect in high dv/dt conditions. These are the exact obstacles that decide whether a 40-stage solid-state Marx generator can deliver nanosecond output pulses with the consistency AWE needs.

A topology under scrutiny

I gave a poster presentation, "Power Electronics-Based High-Voltage Pulse Generation: Design, Simulation, and Hardware Validation of a Solid-State Diode-Clamped Marx Generator", spanning roughly four hours across the two days. After five conferences this year, condensing the project into a short pitch felt natural, and I enjoyed finally going deep on the technical detail with people who wanted it.



The design is a 40-stage diode-clamped topology using 3.3 kV SiC MOSFETs. The headline result was a simulated 10 to 90 percent rise time of 17.41 ns, comfortably inside the sub-30 ns facility requirement, with a 12.59 ns margin left for unmodelled physical delays. To keep that figure honest, I injected 27.7 nH of PCB trace inductance per stage using Wheeler's microstrip expressions and Rosa's partial inductance formula, so the model reflects real parasitics rather than idealised assumptions.

That number drew the sharpest questions. One delegate asked how I reached a 17.41 ns rise time, which let me explain that a simulation is only as realistic as the parasitics you feed it, and that the 12.59 ns margin exists precisely because the model cannot capture everything. Another asked how I balanced pushing switching speed, higher dv/dt, against its downsides, which is exactly what the diode-clamped isolation and 2-ohm bipolar gate drive are there to manage.

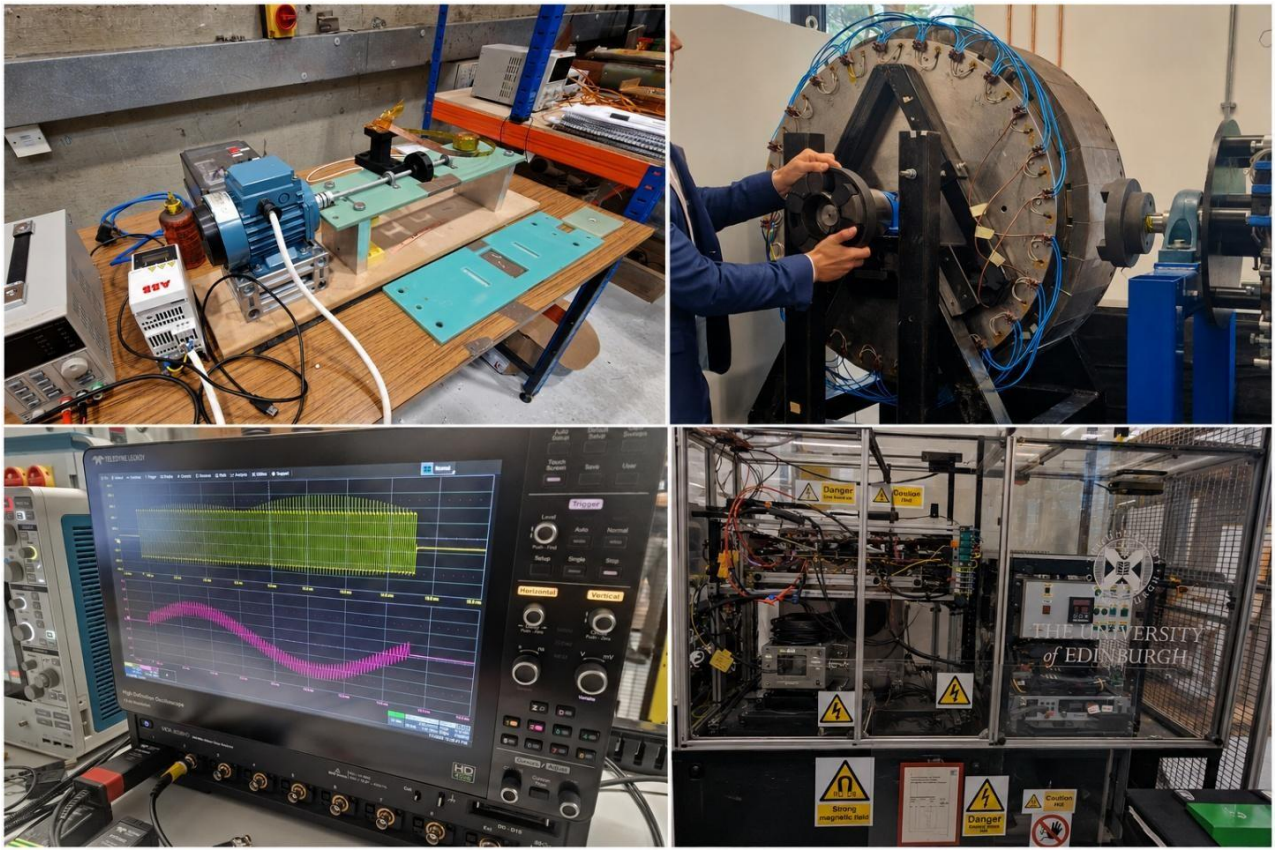
I showed the empirical strand alongside the simulation to keep the methodological boundary clear. A scaled 30 V demonstrator, built from repurposed silicon MOSFETs to stay within university safety limits, confirmed that the parallel-charging and series-erection behaviour of the topology works as predicted before committing to high-voltage SiC parts. Delegates working on prototype validation in wide-bandgap applications were particularly interested in that split.

Networking and technical exchange

Some of the most useful conversations went beyond the poster into the specifics of deploying wide-bandgap semiconductors in national security infrastructure, where qualification and EMI constraints go well past commercial power electronics. We worked through the practical side of critically damped inductive filter networks and the management of reverse-recovery charge in isolation diodes, both live questions for the final hardware iteration. Given the nature of the work, I will keep the detail and the people involved general, but the discussion was a real stress-test of my assumptions rather than polite interest.

A tour of the labs

A tour of the University's power electronics facilities followed, taking in the Wolfson Electrical Power Conversion Laboratory and the associated power electronics and high-temperature semiconductor labs. These sit within Edinburgh's new Engineering Forum at the King's Buildings, opened in April 2026 and part of the Institute for Energy Systems. The Wolfson facility runs a full test service for power conversion and grid equipment at powers up to 240 kW and voltages up to 1500 V, mainly for offshore renewables. Seeing how a test environment at that scale is instrumented and managed was useful context for the high-voltage validation still ahead on my own project.



What the funding made possible

I start a professional engineering role within the Ministry of Defence in September 2026. Presenting this work at a national conference gave me exactly what that transition needs: hard external scrutiny, and the confidence that comes from defending a complex analytical position in front of an informed audience. Specialised pulsed-power research rarely fits a generalist engineering conference. CPE was the right venue because its scope covers the switching dynamics and parasitic management that define this work, and its audience could engage at that level. Without the travel award, presenting to a national audience at this stage would not have been possible. The IET's support bridged the end of my degree and the start of my career, and the dialogue it opened has strengthened both the research and what comes next.

With thanks to the IET and the Postgraduate and Travel Awards Panel.