A SiGe Power Amplifier with Integrated BALUNs for 81-86 GHz E-Band Backhaul Applications

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ABSTRACT

The design of a two-stage differential cascode power amplifier (PA) for 81-86 GHz E-band applications is presented. The PA was realised in SiGe technology with $f_T/f_{\text{max}}$ 170/250 GHz. A broadband transformer with efficiency higher than 79.4% from 71 GHz to 96 GHz is used as a BALUN. The PA delivers a 4.5 dBm saturated output power and exhibits a 13.4 dB gain at 83.6 GHz. The input and output return losses agree well with the design specifications.

INTRODUCTION

Migration to mm-wave frequency regime has proved essential to enabling high-speed data transmission as it provides large bandwidth. For instance, the unlicensed 60 GHz frequency band allocated for short-range indoor applications and the newly licensed E-band aimed for backhaul applications provide at least 5 GHz bandwidth. Traditionally, mm-wave wireless products are realised using III-V technologies such as GaAs and InP thanks to their superior high-frequency performances to silicon technology. Breakthroughs in nanotechnology and optics in the past few years have enabled the production of high-speed transistors in low-cost highly-integrated silicon technology. For example, the maximum oscillation frequency ($f_{\text{max}}$) of SiGe heterojunction bipolar transistors (HBTs) has now exceeded 500 GHz, facilitating development of mm-wave transceivers that include voltage controlled oscillator (VCO), up/down converter, and low-noise amplifier (LNA) as reported in [1]-[3].

The design of mm-wave PA as the most power-hungry building block in the transmitter chain remains one of major challenges, [4]-[7]. While the $f_T$ of the transistors continues to increase thereby enabling higher-frequency operations, the breakdown voltage $BV_{CEO}$ continues to decrease limiting the signal swing and hence reducing the output power. In addition, it is typical for the mm-wave PAs to exhibit rather poor efficiency partly due to lossy passive elements particularly if implemented in low-resistivity silicon substrate.

This paper will describe the design of a two-stage differential cascode PA fabricated in SiGe:C process for 81-86 GHz E-band applications. The design of a low-loss broadband transformer BALUN will also be treated. The complete circuit is illustrated in Fig. 1 and the component values are presented in Table I.

Fig. 1 Schematic of the complete PA
Table I: Circuit Component Values

<table>
<thead>
<tr>
<th>TL_1</th>
<th>( t = 30 , \mu m, w = 5 , \mu m )</th>
<th>C_1</th>
<th>50 fF</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL_2</td>
<td>( t = 70 , \mu m, w = 5 , \mu m )</td>
<td>C_2</td>
<td>55 fF</td>
</tr>
<tr>
<td>TL_3</td>
<td>( t = 70 , \mu m, w = 5 , \mu m )</td>
<td>C_X</td>
<td>60 fF</td>
</tr>
<tr>
<td>TL_4</td>
<td>( t = 60 , \mu m, w = 5 , \mu m )</td>
<td>C_Y</td>
<td>25 fF</td>
</tr>
<tr>
<td>TL_5</td>
<td>( t = 50 , \mu m, w = 5 , \mu m )</td>
<td>C_M</td>
<td>105 fF</td>
</tr>
<tr>
<td>TL_6</td>
<td>( t = 30 , \mu m, w = 5 , \mu m )</td>
<td>C_PAD</td>
<td>25 fF</td>
</tr>
<tr>
<td>TL_M</td>
<td>( t = 180 , \mu m, w = 5 , \mu m )</td>
<td>R_1</td>
<td>250 \Omega</td>
</tr>
<tr>
<td>T_1-T_4</td>
<td>( 0.35 \times 40 , \mu m^2 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Circuit’s Design

Both active and passive circuits are designed using Infineon B7HF200 SiGe process [8]. The HBT transistors are fabricated with a double-polysilicon self-aligned emitter base configuration with a selectively grown SiGe:C base. The peaks of \( f_{\text{max}} \) 170/250 GHz occur at 5 mA/\mu m\(^2\) collector current density. Four copper metal layers (M1–M4) can be used for interconnections as well as for the implementation of passive components. The microstrip lines are realized using the top metal M4 and M2 as the ground plane. The smallest available pad measures 68 \times 68 \mu m\(^2\) and has a parasitic capacitance (C_PAD) of 25 fF. Metal-insulator-metal (MIM) capacitors as well as TaN and polysilicon resistors are also provided in the B7HF200 process.

![Simplified schematic of the driver/PA; (right) 3-D view of the transformer BALUN](image)

The circuit schematic for the driver and the PA is illustrated in Fig. 2. For simplicity, the biasing circuits that allow the amplifier to operate from a single DC supply voltage (VCC) are not included in the schematic. The amplifier employs classic cascode topology, i.e., a common-emitter (CE) T_1-T_2 followed by a common-base (CB) T_3-T_4 in a differential fashion in order to provide sufficient gain as well as to minimize the Miller effect. The cascode stage is emitter degenerated in order to improve bandwidth and to avoid thermal runaway. Input matching element (TL_1-TL_2, C_1-C_2) and output matching element (TL_4-TL_6) are also incorporated on chip. The series capacitance C_1 also functions as a DC-blocking capacitance. The tail current I_BIAS is set to 50 mA in the PA cell and to 16.7 mA in the driver cell.

The 3-D view of the BALUN in Fig. 1 is depicted in Fig. 2. The vertical broadside-coupled structure is adopted here as opposed to the horizontal edge-coupled since it offers higher magnetic coupling factor (k). The differential input coil is realized on M3 while M4 is used for the single-ended output coil. This BALUN is optimized so as to achieve insertion loss as low as practical. Two dominant factors that contribute to the loss mechanism in the BALUN are k and port mismatch. Design parameters that are typically optimized include the transformer radius and the trace width.
The transformer radius is a strong function of the input susceptance and therefore it plays an important role to the port mismatch. The shunt capacitances $C_X$ and $C_Y$, Fig. 1, are added to the input and output ports of the transformer to improve the port mismatch. The transformer radius also determines the self-resonance frequency (SRF), i.e., the smaller the radius, the lower the inductance, the higher the SRF. Meanwhile, the trace width determines the unloaded $Q$-factor of the individual coil self-inductance, i.e., the wider the trace, the lower the parasitic resistance, the higher the $Q$. Ideally, the trace width is set to the maximum metal width allowed by the technology but this may require a larger chip area. After a number of iterative optimizations, the inner radius of the transformer in Fig. 2 is set to 25 $\mu$m and the trace width is set to 5 $\mu$m. The S-parameters of the BALUN obtained from SONNET simulations are plotted in Fig. 3. Here, the single-ended output port (Port 1) is loaded with $C_Y$ in parallel with 50 $\Omega$ resistance whereas the differential input port (Port 2) is terminated with $2C_X$ in parallel with 50 $\Omega$ resistance. Broadband matching with input/output (I/O) return losses higher than 10 dB from 66.5 GHz to 117.5 GHz is achieved. The insertion loss is lower than 1 dB from 71 GHz to 96 GHz. At the centre frequency 83.5 GHz, the loss is 0.85 dB implying 82% efficiency. In contrast, the SiGe transformer BALUN reported in [7] exhibits an extremely high loss of 6.6 dB.

Used as the I/O $\Pi$-type matching element in Fig. 1 is the series microstrip line, $TLM$, which together with the shunt capacitances $C_M$ form a low-pass filter. Fig. 3 shows the simulated return loss and insertion loss of the matching element. At 83.5 GHz centre frequency, the insertion loss is about 1.25 dB.

![Fig. 3 Simulated S-parameter of: (left) the BALUN; (right) the I/O matching circuit](image)

**CIRCUIT’S VALIDATION**

The chip microphotograph of the fabricated PA is shown in Fig. 4. It occupies $1 \times 0.27$ mm$^2$ die area, including RF pads. Each PA/driver cell including the biasing circuits measures $130 \times 260$ $\mu$m$^2$. The amplifier was characterized through on-chip measurements with 100 $\mu$m pitch GSG probes used to probe both input and output ports.

![Fig. 4 Chip microphotograph of the complete PA](image)

For the S-parameter measurements, the circuit was operated from a single VCC $= 2.8$ V. The measured S-parameter results are depicted in Fig. 5. A broadband characteristic is observed where gain $|S_{12}|$ higher than 10 dB is obtained from 71 GHz to 87 GHz. It reaches a peak 13.4 dB at 83.6...
GHz. The I/O return losses are higher than 10 dB from 82 GHz to 88 GHz and from 82 GHz to 95 GHz, respectively. Excellent isolation $|S_{12}|$ higher than 40 dB is achieved. Measured power gain and output power versus input power for VCC = 2.8 V are plotted in Fig. 5. The output power saturates at 4.5 dBm. Actually, the I/O matching elements ($C_M - TL_M - C_M$) in Fig. 1 are not required since the BALUN has been designed to simultaneously match the port impedance that also includes $C_{PAD}$. However, due to the presence of considerable distance between the BALUN and the RF pad, Fig. 4, the $TL_M$ is needed as a routing line. Had these I/O matching elements not existed, the gain and saturated output power would have increased by at least 2.5 dB and 1.25 dB, respectively.

![Fig. 5 Measured: (left) S-parameter; (right) power gain and output power for VCC = 2.8 V](image)

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**REFERENCES**


